

*Amendments to the Claims*

This listing of claims will replace all prior versions, and listings of claims in the application.

Claims 1-7. (Cancelled)

Claim 8. (Currently amended) A superscalar microprocessor for processing instructions having a sequential program order, the microprocessor comprising:

an instruction buffer configured to buffer a plurality of instructions, including at least one conditional branch instruction;

a plurality of functional units configured to execute instructions, thereby generating result data;

a register file including a plurality of entries configured to store data including result data generated by the plurality of functional units;

a ~~decoder~~ resource identifying circuit configured to concurrently identify execution resources for a plurality of buffered instructions, the identified execution resources for each of the plurality of buffered instructions including a functional unit capable of executing the instruction and a register file entry corresponding to a source of an operand for the instruction,

wherein the ~~decoder~~ resource identifying circuit is further configured to make a group of at least two and not more than a maximum number N of instructions

concurrently available for execution, wherein the group may include up to N conditional branch instructions;

an issue control circuit coupled to the ~~decoder~~ resource identifying circuit and configured to concurrently issue more than one of the available instructions to the functional units for execution, based on availability of the identified execution resources for each instruction identified by the decoder circuit and without regard to the sequential program order; and

a plurality of data routing paths coupled between the plurality of functional units and the register file and configured to concurrently transfer result data from more than one of the plurality of functional units to the register file.

Claim 9. (Currently amended) The microprocessor of claim 8, further comprising:

bypass control logic coupled to the plurality of data routing paths and configured to ~~supply~~ distribute result data from a first one of the plurality of functional units as operand data for any one or more of the plurality of functional units via an alternate data path that bypasses the register file,

wherein ~~supplying~~ distributing result data via the alternate data path occurs concurrently with transferring result data to the register file.

Claim 10. (Previously presented) The microprocessor of claim 8, further comprising an instruction fetch unit configured to fetch instructions from an instruction

store according to the sequential program order and to transfer fetched instructions to the instruction buffer.

Claim 11. (Previously presented) The microprocessor of claim 8, wherein the instruction fetch unit includes a branch prediction circuit configured to detect a conditional branch instruction among the fetched instructions and to generate a branch bias signal indicating whether the conditional branch is predicted to be taken or not taken.

Claim 12. (Previously presented) The microprocessor of claim 11, wherein the instruction fetch unit is further configured to select an instruction to be transferred to the instruction buffer subsequent, in the sequential program order, to the conditional branch instruction based at least in part on the branch bias signal.

Claim 13. (Previously presented) A method for processing instructions having a sequential program order in a superscalar microprocessor, the method comprising:

buffering a plurality of instructions, including at least one conditional branch instruction;

concurrently identifying execution resources for more than one of a plurality of buffered instructions, the identified execution resources for each of the plurality of buffered instructions including a functional unit capable of executing the instruction and a register file entry corresponding to a source of an operand for the instruction;

making a group of at least two and not more than a maximum number N of instructions for which execution resources have been identified concurrently available for execution, wherein the group may include up to N conditional branch instructions;

concurrently issuing more than one of the group of available instructions for execution by a plurality of functional units, based on availability of the identified execution resources for each instruction and without regard to the sequential program order;

executing the issued instructions in the plurality of functional units, thereby generating result data; and

transferring the result data from the functional units to a register file, the register file including a plurality of entries.

Claim 14. (Previously presented) The method of claim 13, further comprising, concurrently with the act of transferring, bypassing the result data from a first one of the plurality of functional units as operand data for any one or more of the plurality of functional units.

Claim 15. (Previously presented) The method of claim 13, further comprising fetching instructions from an instruction store according to the sequential program order.

Claim 16. (Previously presented) The method of claim 15, further comprising:  
detecting a conditional branch instruction among the fetched instructions;  
and

generating a branch bias signal indicating whether the conditional branch is predicted to be taken or not taken.

Claim 17. (Previously presented) The method of claim 16, wherein the act of buffering a plurality of instructions includes selecting and buffering an instruction that is subsequent, in the sequential program order, to the conditional branch instruction, wherein the selection is based at least in part on the branch bias signal.

Claim 18. (Currently amended) A computer system, comprising:

a memory;

a superscalar microprocessor for processing instructions having a sequential program order; and

a bus coupled between the memory and the microprocessor,

wherein the microprocessor includes:

an instruction buffer configured to buffer a plurality of instructions, including at least one conditional branch instruction;

a plurality of functional units configured to execute instructions, thereby generating result data;

a register file including a plurality of entries configured to store data including result data generated by the plurality of functional units;

a ~~decoder~~ resource identifying circuit configured to concurrently identify execution resources for a plurality of buffered instructions, the identified execution resources for each of the plurality of buffered instructions including a functional unit

capable of executing the instruction and a register file entry corresponding to a source of an operand for the instruction,

wherein the ~~decoder~~ resource identifying circuit is further configured to make a group of at least two and not more than a maximum number N of instructions concurrently available for execution, wherein the group may include up to N conditional branch instructions;

an issue control circuit coupled to the ~~decoder~~ resource identifying circuit and configured to concurrently issue more than one of the available instructions to the functional units for execution, based on availability of the identified execution resources ~~identified by the decoder circuit~~ for each instruction and without regard to the sequential program order; and

a plurality of data routing paths coupled between the plurality of functional units and the register file and configured to concurrently transfer result data from more than one of the plurality of functional units to the register file.

19. (Currently amended) The system of claim 18, wherein the microprocessor further includes:

bypass control logic coupled to the plurality of data routing paths and configured to ~~supply~~ distribute result data from a first one of the plurality of functional units as operand data for any one or more of the plurality of functional units via an alternate data path that bypasses the register file,

wherein ~~supplying~~ distributing result data via the alternate data path occurs concurrently with transferring result data to the register file.

20. (Previously presented) The system of claim 18, wherein the microprocessor further includes an instruction fetch unit configured to fetch instructions from an instruction store according to the sequential program order and to transfer fetched instructions to the instruction buffer.

21. (Previously presented) The system of claim 20, wherein the instruction fetch unit includes a branch prediction circuit configured to detect a conditional branch instruction among the fetched instructions and to generate a branch bias signal indicating whether the conditional branch is predicted to be taken or not taken.

22. (Previously presented) The system of claim 21, wherein the instruction fetch unit is further configured to select an instruction to be transferred to the instruction buffer subsequent, in the sequential program order, to the conditional branch instruction based at least in part on the branch bias signal.

Claim 23. (Previously presented) The microprocessor of claim 8, further comprising retirement control logic coupled to the register file and configured to concurrently retire a plurality of instructions according to the sequential program order.

Claim 24. (Previously presented) The method of claim 13, further comprising retiring instructions according to the sequential program order.

Claim 25. (Previously presented) The computer system of claim 18, wherein the microprocessor further includes retirement control logic coupled to the register file and configured to concurrently retire a plurality of instructions according to the sequential program order.

Claim 26. (New) The microprocessor of claim 8, wherein the resource identifying circuit is further configured to concurrently identify execution resources for a first one and a second one of the plurality of buffered instructions, wherein the second one of the instructions has a data dependency on the first one of the instructions.

Claim 27. (New) The method of claim 13, wherein concurrently identifying execution resources for more than one of the plurality of buffered instructions includes concurrently identifying execution resources for a first one and a second one of the plurality of buffered instructions, wherein the second one of the instructions has a data dependency on the first one of the instructions.

Claim 28. (New) The system of claim 18, wherein the resource identifying circuit is further configured to concurrently identify execution resources for a first one and a second one of the plurality of buffered instructions, wherein the second one of the instructions has a data dependency on the first one of the instructions.